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Search History

DATE: Monday, January 24, 2005 Printable Copy Create Case

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L5	L4 and (electrical adj path)	28	L5
L4	L3 and (second near3 (drain))	2777	L4
L3	L2 and (second near3 (source))	3892	L3
L2	L1 and (second near4 conductivity)	9316	L2
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☐ 1. Document ID: US 6521923 B1

L7: Entry 1 of 7 File: USPT Feb 18, 2003

US-PAT-NO: 6521923
DOCUMENT-IDENTIFIER: US 6521923 B1

TITLE: Microwave field effect transistor structure on silicon carbide substrate

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 2. Document ID: US 6147538 A

L7: Entry 2 of 7 File: USPT Nov 14, 2000

US-PAT-NO: 6147538
DOCUMENT-IDENTIFIER: US 6147538 A
** See image for Certificate of Correction **

TITLE: CMOS triggered NMOS ESD protection circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 3. Document ID: US 5929469 A

L7: Entry 3 of 7 File: USPT Jul 27, 1999

US-PAT-NO: 5929469
DOCUMENT-IDENTIFIER: US 5929469 A

TITLE: Contact holes of a different pitch in an application specific integrated circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 4. Document ID: US 5874754 A

L7: Entry 4 of 7 File: USPT Feb 23, 1999

US-PAT-NO: 5874754
DOCUMENT-IDENTIFIER: US 5874754 A

TITLE: Microelectronic cells with bent gates and compressed minimum spacings, and method of patterning interconnections for the gates

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 5. Document ID: US 5796130 A

L7: Entry 5 of 7 File: USPT Aug 18, 1998

US-PAT-NO: 5796130
DOCUMENT-IDENTIFIER: US 5796130 A

TITLE: Non-rectangular MOS device configurations for gate array type integrated circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 6. Document ID: US 5440154 A

L7: Entry 6 of 7 File: USPT Aug 8, 1995

US-PAT-NO: 5440154
DOCUMENT-IDENTIFIER: US 5440154 A

TITLE: Non-rectangular MOS device configurations for gate array type integrated circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 7. Document ID: US 4612629 A

L7: Entry 7 of 7 File: USPT Sep 16, 1986

US-PAT-NO: 4612629
DOCUMENT-IDENTIFIER: US 4612629 A

TITLE: Highly scalable dynamic RAM cell with self-signal amplification

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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L7: Entry 1 of 7 File: USPT Feb 18, 2003

US-PAT-NO: 6521923
DOCUMENT-IDENTIFIER: US 6521923 B1

TITLE: Microwave field effect transistor structure on silicon carbide substrate

DATE-ISSUED: February 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
D'Anna; Pablo	Redding	CA		
Johnson; Joseph H.	Phoenix	AZ		

US-CL-CURRENT: 257/288; 257/213, 257/275, 257/285, 257/341, 257/368, 257/389, 257/508, 257/E21.538, 257/E29.119, 257/E29.268

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L7: Entry 2 of 7 File: USPT Nov 14, 2000

DOCUMENT-IDENTIFIER: US 6147538 A
** See image for Certificate of Correction **
TITLE: CMOS triggered NMOS ESD protection circuit

Brief Summary Text (6):
A second source of ESD is from metallic objects, and is known as the machine model (MM) ESD source. The MM ESD source is characterized by a greater capacitance and lower internal resistance than the HBM ESD source. The MM ESD model can result in ESD transients with significantly higher rise times than the HBM ESD source.

Brief Summary Text (9):
In MOS integrated circuits, the inputs are normally connected to drive the gate of one or more MOS transistors. The term "MOS" is used in this application, as is now conventional, to refer to any insulated-gate-field-effect-transistor, or to integrated circuits which include such transistors. Furthermore, all pins are provided with protective circuits to prevent voltages from damaging the MOS gates. These protective circuits, normally placed between the input and output pads on a chip and the transistor gates to which the pads are connected, are designed to begin conducting, or to undergo breakdown, thereby providing an electrical path to ground (or to the power-supply rail) when excess voltage occurs. Such protection devices are designed to avalanche (passing a large amount of current, and dissipating the energy of the incoming transient) before the voltage on the input pin can reach levels which would damage the gate oxide. Since the breakdown mechanism is designed to be nondestructive, the protective circuits provide a normally open path that closes only when the high voltage appears at the input or output terminals, harmlessly discharging the node to which it is connected.

Brief Summary Text (10):
However, technological advances are leading to the creation of smaller and faster components that are increasingly more fragile. The output stages of MOS circuits which, until now, have been capable of withstanding high discharge currents, are becoming more vulnerable. In particular, the advantages of the various techniques for improving the performance characteristics of integrated circuits are offset by increased sensitivity to over-voltages or discharges. Breakdown voltages of the junctions or punch-through voltages between drain and source of the MOS transistors are becoming lower and the gate oxide is more fragile.

Brief Summary Text (11):
ESD protection for MOS output buffers has typically relied on a parasitic lateral bipolar transistor of the MOS devices. When the voltage reaches the breakdown voltage of the devices, the lateral transistors should turn on and clamp the pad voltage at a sufficiently low voltage to protect the output buffer. The devices typically have a snap-back characteristic during breakdown. The parasitic transistor triggers at a high voltage and snaps-back to a lower voltage to clamp the pad voltage. However, a portion of the MOS device can trigger and snap-back to a lower voltage and conduct all of the current. When this happens, this part can be destroyed before the voltage rises high enough to trigger the rest of the device. This is especially a problem for devices with low resistance substrates, since the substrate is the base of the parasitic lateral transistors and the base is difficult to forward bias if it is low resistance. Low resistance substrates are

desirably used on CMOS circuits to prevent latchup of parasitic SCRs in normal operation, however, this conflicts with the use of SCRs for ESD protection.

Brief Summary Text (12):
As integrated circuits (ICs) become more complicated and, as a result, denser, the metal-oxide-semiconductor (MOS) circuit elements that make up the IC must become smaller. As the size of a MOS circuit element shrinks, its operating voltage also tends to drop. In the past, the standard operating voltage of MOS circuit elements was 5 V. Newer designs are using operating voltages in the 2.5 to 3.3 volt range. For compatibility, it is desirable for the newer designs to be able to withstand 5 V signals. Unfortunately, technologies developed for 3 V operation have thin gate oxides, on the order of 100 angstroms. If a thin oxide device designed for 3 V operation were instead operated at 5 V, the device would have accelerated wear-out due to reduced gate oxide reliability.

Brief Summary Text (13):
ESD protection circuits using MOS circuit elements must be designed to avoid having the oxides stressed by a 5 V bond pad voltage during normal operation. At the same time, the protection circuit must turn-on and provide good ESD protection during ESD stress. One prior art solution uses two gate oxide thicknesses. A thinner oxide is used for the internal functional circuitry and a thicker oxide is used for circuitry connected directly to a bond pad. Unfortunately, this adds process complexity by requiring two gate oxide formations. Thus, there is a need for ESD protection circuitry that will not be stressed during 5 V operation and that minimizes process complexity.

Brief Summary Text (17):
In general, and in an embodiment of the present invention, an integrated circuit is provided with ESD protection circuitry having amplifier circuitry to increase substrate pump current in response to an ESD event. The integrated circuit has a semiconductor substrate with a bond pad for a reference supply voltage and a signal bond pad for connecting to an external signal. The ESD circuitry is connected between the signal pad and the reference supply voltage bond pad. The ESD circuitry has a substrate region in the semiconductor substrate enclosed by a highly doped region, with a first MOS transistor of a first conductivity type with a backgate in the first substrate region, a first source/drain connected to the signal bond pad, a second source/drain connected to the reference supply voltage bond pad, and a control gate connected to the highly doped region. There is a complimentary triggering MOS transistor of a second conductivity type with a first source/drain connected to the signal bond pad, a second source/drain connected to the highly doped region, and a control gate. Control circuitry is connected to the first signal bond pad and to the control gate of the second MOS transistor and is operable to provide a control signal to the control gate of the complimentary triggering MOS transistor in response to an ESD zap applied to the first signal bond pad.

Brief Summary Text (18):
In accordance with another aspect of the present invention, a second triggering MOS transistor has a first source/drain connected to the signal bond pad, a second source/drain connected to the control gate of the second MOS transistor, and a control gate connected to the complimentary triggering transistor.

Brief Summary Text (20):
In accordance with another aspect of the present invention, the first MOS transistor and the triggering MOS transistor can be cascode connected transistors.

Detailed Description Text (11):
FIG. 2 illustrates graphs of current (I) (in milliamps) vs. voltage (in volts, V) of a typical I-V breakdown characteristic for an NMOS transistor under different gate bias conditions as measured in a TLP system with a 200 ns pulse width. Vt1 is

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☐ 1. Document ID: US 6521923 B1

L3: Entry 1 of 2 File: USPT Feb 18, 2003

US-PAT-NO: 6521923
DOCUMENT-IDENTIFIER: US 6521923 B1

TITLE: Microwave field effect transistor structure on silicon carbide substrate

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 2. Document ID: US 6372557 B1

L3: Entry 2 of 2 File: USPT Apr 16, 2002

US-PAT-NO: 6372557
DOCUMENT-IDENTIFIER: US 6372557 B1

TITLE: Method of manufacturing a lateral fet having source contact to substrate with low resistance

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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